CUSTOMER NO. 23932

Docket No.: 64476-00002USPX
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Vivek Nautiyal et al.

Application No.: 10/684076 — Confirmation No.: 3058

Filed: October 10, 2003 — Art Unit: 2816

For: SENSE AMPLIFIER WITH FEEDBACK-CONTROLLED BITLINE ACCESS — Examiner: L. T. Nguyen

CLAIM FOR PRIORITY AND SUBMISSION OF DOCUMENTS

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Dated: September 16, 2004 Signature: _____
(Mario Barbarash)

Dear Sir:

Applicant hereby claims priority under 35 U.S.C. 119 based on the following prior foreign application filed in the following foreign country on the date indicated:

Country	Application No.	Date
India	1039/Del/2002	October 16, 2002

In support of this claim, a certified copy of the said original foreign application is filed herewith.

Dated: September 16, 2004

Respectfully submitted,

By _____
Andre M. Szuwalski
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IFW

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PTO/SB/21 (04-04)
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/684076-Conf. #3058
Filing Date	October 10, 2003
First Named Inventor	Vivek Nautiyal
Art Unit	2816
Examiner Name	L. T. Nguyen
Total Number of Pages in This Submission	
Attorney Docket Number	64476-00002USPX

ENCLOSURES (*Check all that apply*)

- [ ] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [x] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance communication to Technology Center (TC)
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):

  Claim of Priority;
  Return Receipt Postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	JENKENS & GILCHRIST, A PROFESSIONAL CORPORATION Andre M. Szuwalski 35,701
Signature	
Date	September 16, 2004

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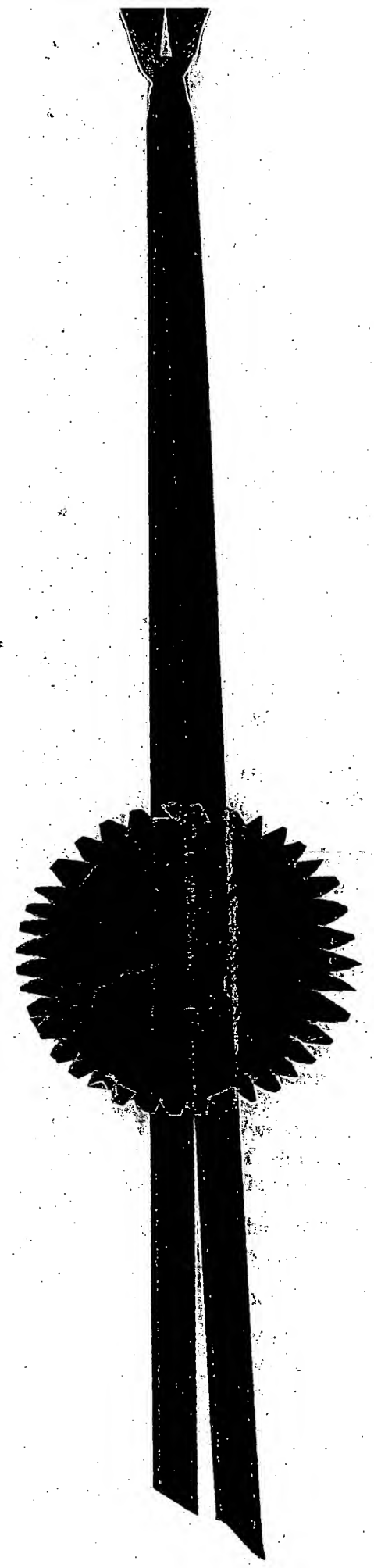

सत्यमेव जयते

INTELLECTUAL PROPERTY INDIA

GOVERNMENT OF INDIA
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PATENT OFFICE, DELHI BRANCH,
W - 5, WEST PATEL NAGAR,
NEW DELHI - 110 008.

I, the undersigned, being an officer duly authorized in accordance with the provision of the Patent Act, 1970 hereby certify that annexed hereto is the true copy of the ***Application, Complete Specification*** *and* ***Drawing Sheets*** *filed in connection with Application for Patent No.* ***1039/Del/02*** *dated* ***16th October 2002.***

Witness my hand this 24th Day of October 2003.

(S.K. PANGASA)
Assistant Controller of Patents & Designs

CERTIFIED COPY OF PRIORITY DOCUMENT

FORM 1

THE PATENTS ACT, 1970

(39 of 1970)

APPLICATION FOR GRANT OF A PATENT

(See Sections 5(2), 7, 54 and 135)

16 OCT 2002

1. I/we,

STMicroelectronics Pvt. Ltd., an Indian company, of Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 3001, Uttar Pradesh, India.

2. hereby declare –

(a) that I am/we are in possession of an invention titled ***"An Improved Sense Amplifier."***

(b) that the ~~provisional~~ / complete specification relating to this invention is filed with this application

(c) that there is no lawful ground of objection to the grant of a patent to me/us.

3. further declare that the inventor(s) for the said inventions is/are

(i) NAUTIYAL Vivek, an Indian citizen, of Deep Villa, Balasaur Kotdwara, District Garhwal, U.P., India.

(ii) KUMAR Ashish, an Indian citizen, of M-17 Housing Colony, Ranchi – 834009, Bihar, India.

4. I/we claim the priority from the application(s) filed in convection countries, particulars of which are as follows: **NA**

5. I/we state that the said invention is an improvement in or modification of the invention the particulars of which are as follows and of which I/we are the applicant/patentee: **NIL**

6. I/we state that the application is divided out of my/our application, the particulars of which are given below and pray that this application be deemed to have been filed on under section 16 of the Act. **NIL**

7. That I am/we are the assignee or legal representative of the true and first inventors.

8. That my/our address for service in India is as follows:

ANAND & ANAND, Advocates
B-41, Nizamuddin East
New Delhi – 110 013

Tel Nos.: (11) 4355078, 4355076, 4350360
Fax Nos.: (11) 4354243, 4352060

9- I/We the true and first inventors of this invention or the applicant(s) in the convention country declare that the applicant(s) herein is/are my/our assignee or legal representative.

a) *VIVEK NAUTIYAL an Indian National of DEEP VILLA, BALASAUR KOTDWARA, DISTRICT :- GARHWAL , U.P.*

Signature

Dated this 16th day of October 2002

b) *ASHISH KUMAR an Indian National of M-17 Housing Colony, Ranchi-834009*

Signature

Ashish Kumar

Dated this 16th day of October 2002

10- that to the best of my/our knowledge, information and belief the fact and matters stated herein are correct and that there is no lawful ground of objection to grant of patent to me/us on this application.

11- Following are the attachment with the application

(a) Complete specification (3 copies)
(b) Abstract
(c) Formal drawings
(d) Power of Attorney
(e) Form 1 (in triplicate)
(f) Form 3 (in duplicate)
(g) Fee Rs. 5000/- In cash/cheque/bank draft bearing no. , date On Bank.

I/We request that a patent may be granted to me/us for the said invention.

Dated this 16th day of October 2002

Signature
STMicroelectronics Pvt. Limited

02-IND-138

Form 2

THE PATENTS ACT, 1970

16 OCT 2002

COMPLETE SPECIFICATION

SECTION 10

'AN IMPROVED SENSE AMPLIFIER'

***STMicroelectronics Pvt. Ltd.**, Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 3001, Uttar Pradesh, India, an Indian Company*

The following specification particularly describes and ascertains the nature of this invention and the manner in which it is to be performed:

AN IMPROVED SENSE AMPLIFIER

Field of the Invention

This invention relates to an improved sense amplifier with feedback-controlled bitline-access.

Background of the Invention

The Sense amplifier shown in **figure 1** is the most common sense amplifier topology in SRAM and DRAM cells. The function of a sense amplifier in a DRAM is to amplify the signal and to restore the levels on the bit lines to the full logic level since the read operation in a one-transistor cell is destructive. In SRAMs, the use of a sense amplifier offers performance enhancements. The sense amplifier can be used to speed up the access since the bit lines do not have to swing to their full value by discharging through the cell. The sense amplifier transistors can be made quite large compared to the cell transistors to drive the bit lines to full logic level quickly.

A sense amplifier amplifies the data signals in either a normal mode or an altered mode. In the normal mode, the data signals must be complementary to each other while in the altered mode, the data signals need not be complementary to each other. In the normal mode, a mode control circuit couples each of the data signals to a respective second input of each sense amplifier so that each sense amplifier receives complimentary data signals at its differential inputs. In the altered mode, the mode control circuit couples a reference voltage to the second inputs of the sense amplifier in the first stage so that each sense amplifiers compares a respective data signal to the reference voltage. Normal mode sense amplifiers are commonly used for high speed SRAM's. Access to bitline is provided to the evaluating nodes. The sense amplifier enable signal is used for initiating latching operation and disconnecting the bitlines during the evaluation phase.

Figure 1 shows the schematic circuit diagram of a conventional normal mode latch type sense amplifier. The circuit consists of p-type MOS transistors **M11, M12** and n-type MOS transistors **M13, M14** such that they form a data latch. The data latch is provided with an enabling/disabling MOS transistor **M15** such that when the MOS transistor **M15** is enabled it provides a path to the power supply to complete the circuit.

The data latch is accessed by bitlines **BL,** and **BLB** through MOS transistors **M16** and **M17.** MOS transistors **M15, M16** and **M17** are provided with control signal **SAEN** at their gates such that when the access MOS transistors **M16** and **M17** are enabled MOS transistor **M15** remains disabled and vice versa. Signal nodes **SN1** and **SN2** are the evaluating nodes of the latch. A MOS transistor **M18** is connected between nodes **SN1** and **SN2** of the latch. The gate of **M18** is connected to Sense Amplifier Equalizing signal **SAEQ**. After wordline selection, one of the bitline discharges through memcell. When a sufficient amount of voltage split is available at the latch nodes, signal **SAEN** disables access transistors **M16** and **M17** and thereby disconnects the bitlines from the evaluating nodes, while at the same time enabling transistor M15 provides a ground path for the latching operation.

In a conventional sense amplifier, undesired noise is generated at the sense amplifier nodes when the accessed device is switched off through senseamp enable signal. Also the input nodes of a conventional sense amplifier are disconnected to the bitlines during the evaluation stage, which disables the additional load on sense amplifier nodes due to charge injection from bit lines. Noise generated at the sense amplifier nodes delays the evaluation.

The Objects and Summary of the Invention

The object of the invention is to obviate the above drawback while minimizing the extra load due to bitline charge injection.

Another object of the invention is to provide a faster sense amplifier.

It is another object of the invention to obviate undesired noise generation at the sense amplifier nodes, by providing a feedback at the bitline and the signal nodes that enables dynamic sampling during evaluation.

Yet another object of the invention is to provide a reliable sense amplifier.

To achieve these objectives the invention provides a novel feedback controlled bit line access scheme, utilizing optimum bit line assistance during the evaluation phase. The feedback ensures automatic control of the amount of bitline assistance taken with the process mismatch (Due to device as well as interconnect capacitance mismatch) present in the sense amplifier. Variations due to process mismatch present in the sense-amplifier transistors, result in

delayed evaluation with corresponding best-case evaluation and worst-case evaluation times. Self- timed operation (feedback controlled access) ensures the overload due to bitline charge injection is optimum for all the cases. In case of small mismatch between sense amplifier nodes, the evaluation is fast and the bitline charge injection is small. In the case of large mismatches the evaluation is delayed and the amount of charge injected is large. This arrangement provides reliable operation of sense amplifier.

An inverter feedback is also provided to further assist the evaluating nodes.

Brief Description of the Accompanying Drawings

The invention will now be described with reference to the accompanying drawings.

Figure 1 shows a schematic circuit diagram of a conventional latch type sense amplifier.

Figure 2 shows a schematic circuit diagram in accordance with the present Invention using inverter feedback.

Figure 3 shows a schematic circuit diagram in accordance with an embodiment of the present invention.

Detailed Description

Figure 1 has already been described under the heading 'Background of the invention'.

Figure 2 shows a schematic circuit diagram in accordance with the present invention. PMOS transistors **M21, M22** and NMOS transistors **M23, M24** form the latch of a sense amplifier. The gate of the equalizing PMOS transistor **M212** is connected to Sense Amplifier Equalize Signal **SAEQ**. Bitlines **BL** and **BLB** are connected through PMOS transistors **M26** and **M27** to the latch. The gate of the latch-enabling transistor **M25** is connected to control signal **SAEN**. The outputs of inverters **INV1, INV2** are fedback to gates of access transistors **M26, M27** from evaluating nodes **SN1, SN2** respectively.

As an example, before the start of read operation both the bitlines are precharged to high, sense amplifier nodes SN1 and SN2 are also initially precharged, access transistors M26 and M27 connects the SN1 and SN2 to BL and BLB respectively. When wordline is enabled one

of the bitline say BL starts discharging through the memcell and so the sense amplifier node SN1, When SAEN signal enables nMOS transistor M25 the latching action is initiated. As soon as evaluation takes place feedback from **SN1** switches off access transistor **M26** and dynamically disconnects the additional load due to charge injection by the bitline. Any undesired noise generation at the sense amplifier nodes is suppressed in the present invention by providing feedback, to enable dynamic sampling during evaluation.

Since this method takes optimum assistance of bitline discharges, it does not introduce any extra overhead on the overall sensing time and hence results in faster sensing.

The present invention utilizes the continuously discharging bitlines during evaluation, accommodating the delay overhead due to bitline charge injection over the relaxation time of generated noise.

A person ordinarily skilled in the art will appreciate that the feedback-controlled access can be realized in many ways. One out of many possible embodiments is the inverter feedback controlled access as discussed above.

The advantage of using inverter feedback is that it provides controlled access as the high going node is continuously connected to the bitline whereas the low going node is disconnected. In this case equalization after the first read is facilitated by bitline thereby enabling quick operation. Further, since the high going node is continuously connected to bitline the pull up PMOS in the latch may be kept small thereby compensating for the area taken by extra circuitry added in the scheme.

The invention also provides for the early switching off of the evaluating NMOS (high going node). The feedback speeds up the evaluation process and also adds to the stability and reliability of the sense-amp. MOS transistors **M28**, **M210** form inverter **A** and the MOS transistors **M29**, **M211** form inverter **B**. The Source of the NMOS transistors in inverter **A** and inverter **B** are connected to the drain of enabling NMOS transistor **M25**. Nodes **SN2**, **SN1** are fed as inputs to inverters **A** and **B** respectively. The output of inverter **A** is connected to the source of NMOS transistor **M23**, while the output of inverter **B** is connected to the source of NMOS transistor **M24**. Inverter B facilitates the discharging of node **SN1** and helps

in switching off NMOS transistor **M24** thereby speeding-up the evaluation process while also improving the stability of the sense amp.

The sense amplifier provided with feedback controlled access alone and the sense amplifier provided with feedback inverter can be used separately or in combination depending upon the requirement and chip area constrains.

Figure 3 show a schematic circuit diagram in accordance with another embodiment of the present invention using NAND gate feedback controlled access. The NAND gate feedback controlled access sense amplifier can be easily realized by removing the **INV1** and **INV2** from **Figure 2** and by connecting the gates of the access enabling MOS transistors to the output of a NAND gate, and connecting the inputs of the NAND gate to nodes **SN1, SN2** as shown.

In this case a completion signal is generated immediately after the evaluation and may be used as control signal for many purposes, such as wordline disabling.

Accordingly, this invention is not to be considered limited to the specific examples chosen for purposes of disclosure, but rather to cover all changes and modifications, which do not constitute departures from the permissible scope of the present invention. The invention is therefore not limited by the description contained herein or by the drawings, but only by the claims.

We Claim:

1. An improved sense amplifier comprising:
   - cross-coupled inverters forming a latch,
   - an enabling/disabling means connected between the common supply terminal and a common conducting terminal of the latch,
   - access control transistors connected between the access lines and the output nodes of the latch, and
   - a first equalizing means to connect both outputs of the latch

   characterized in that it includes,
   - a feedback means connected from the output nodes of the latch to the control terminals of the access control transistors,
   - the outputs of a second set of inverters connected to the conducting terminals of said latch, with the inputs of the second set of inverters connected to the inputs of said latch, and the enabling/disabling means connected between the conducting terminals of the second set of inverters and the supply terminals, and
   - a second equalizing means connected to the said common conducting lines of the said latch,

   to provide increased speed of operation and improved reliability.

2. An improved sense amplifier as claimed in claim 1 wherein the sense amplifier is realized using either a feedback means or with a second set of inverters or with the combination of both.

3. An improved sense amplifier as claimed in claim 1 wherein the enabling/disabling means is a MOS transistor.

4. An improved sense amplifier as claimed in claim 1 wherein the first and second equalizing means are a pair of MOS transistors with their control terminals (GATEs) tied together.

5. An improved sense amplifier as claimed in claim 1 wherein the feedback control means is an inverter.

6. An improved sense amplifier as claimed in claim 1 wherein the feedback control means is a NAND gate with inputs connected to the output nodes and its output connected to the control terminals of the access control transistors.

7. An improved sense amplifier substantially as herein described with reference to and as illustrated in figures 2 & 3 of the accompanying drawings.

Dated this 16th day of Oct, 2002

Shanti Kumar

of **ANAND & ANAND, Advocates**
Agents for the Applicants

ABSTRACT

This invention relates to a novel feedback controlled bit line access scheme, utilizing optimum bit line assistance during the evaluation phase. The feedback ensures automatic control of the amount of bitline assistance taken with the process mismatch (Due to device as well as interconnect capacitance mismatch) present in the sense amplifier. Variations due to process mismatch present in the sense-amplifier transistors, result in delayed evaluation with corresponding best-case evaluation and worst-case evaluation times. Self- timed operation (feedback controlled access) ensures the overload due to bitline charge injection is optimum for all the cases. In case of small mismatch between sense amplifier nodes, the evaluation is fast and the bitline charge injection is small. In the case of large mismatches the evaluation is delayed and the amount of charge injected is large. This arrangement provides reliable operation of sense amplifier.

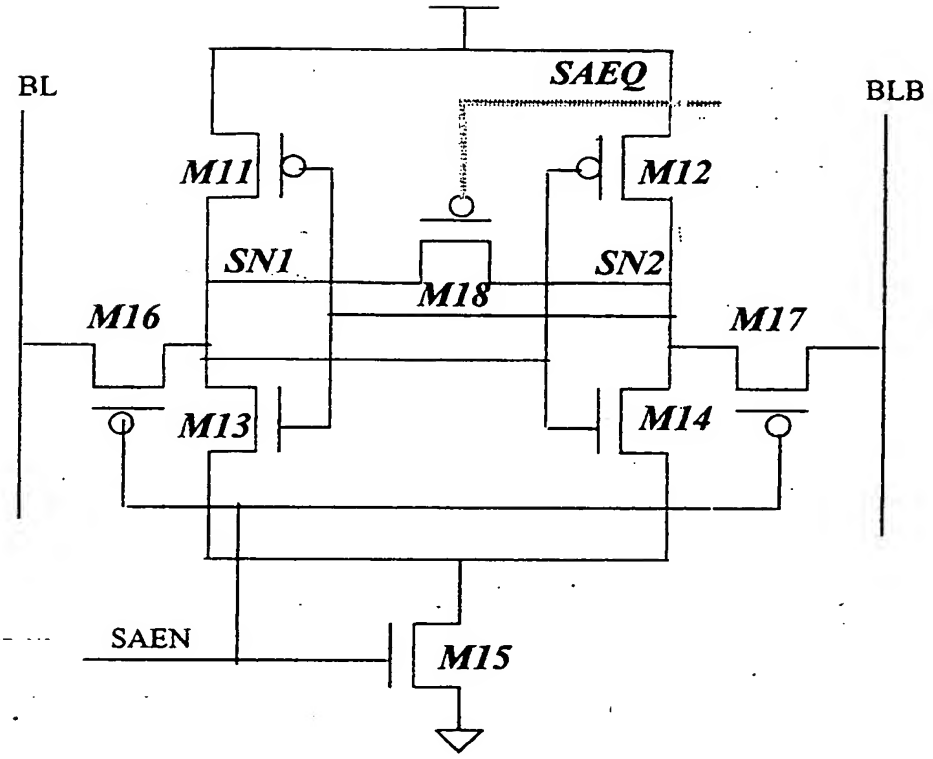

FIG 1
(CONVENTIONAL)

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Attorney for the Applicant

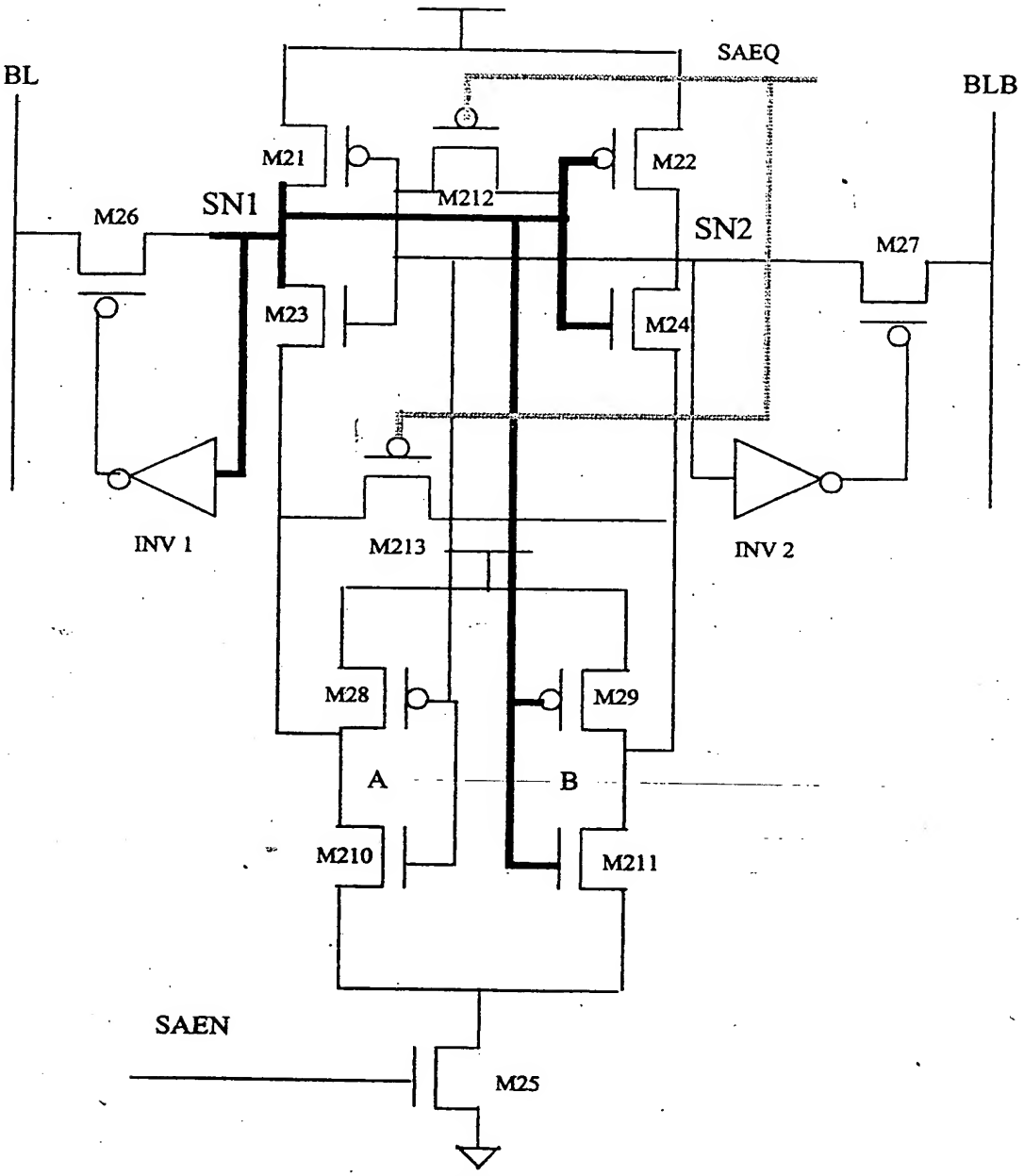

Figure-2
Proposed scheme with inverter feedback

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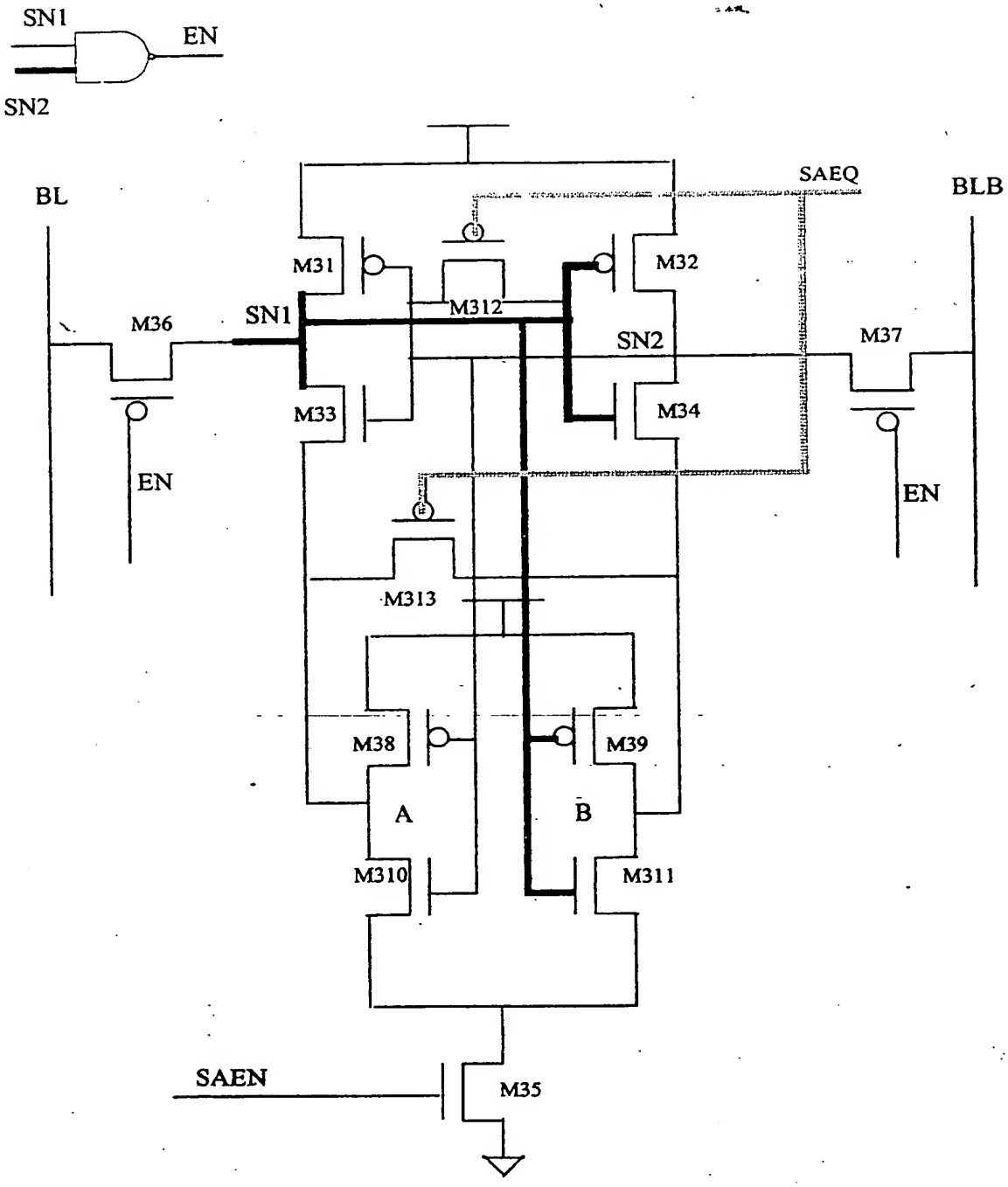

Figure-3
Proposed scheme with NAND feedback

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